REMARKS

This paper is responsive to the Office Action of December 4, 2002. Reexamination and reconsideration of the application are respectfully requested.

The Office Action

Claims 1-4, 8, 9 and 20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Wilting (U.S. Pat. No. 4,080,719).

Claims 1-5, 8, 9 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Grant et al. (U.S. Pat. No. 6,423,619) in view of Wilting.

Claims 6 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Grant in view of Wilting and further in view of Raajimakers et al. (U.S. Pat. Application Pub. No. US 2001/0031562A1).

Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Wilting in view of Venkatesan et al. (U.S. Pat. No. 5,736,435).

Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Grant in view of Wilting and further in view of Venkatesan et al.

Drawings

The applicants gratefully acknowledge the acceptability of the drawings filed on January 11, 2002.

The Present Claims Distinguish Patentably Over the References of Record

As a brief review, the present invention is directed to a semiconductor device including a source and a drain, which consist essentially of silicide, and a gate dielectric made from a high-K dielectric material (i.e., a dielectric material having a relative permittivity greater than 10). The silicide source and drain are formed by reacting a metal layer 74 with a layer of semiconductor material 18 such that the source and drain are

formed without the use of conventional ion implantation. Forming a semiconductor device, having a silicide source and drain and a high-K gate dielectric, without conventional ion implantation, provides a device with improved structure and performance.

In contrast, conventional semiconductor devices are formed with conventional ion implantation (e.g., the devices disclosed in Wilting and Grant) to form source and drain regions. Ion implantation is usually followed by one or more associated anneal cycles to activate those dopant species and/or to recrystalize the layer of semiconductor material.

These additional anneal cycles can adversely affect the structural features and integrity of the device. For example, the additional thermal processing associated with the conventional device may exceed the thermal budget of one or more materials in the device, such as the gate dielectric material, which could lead to the material becoming unstable, the material losing its electrical characteristics, and/or an undesirable reaction with other materials in the device.

In particular, high-K dielectric materials (i.e., as defined in the specification, materials having a dielectric constant of greater than 10 or greater than 20) are often sensitive to excessive thermal processing, thereby limiting the thermal budget. Therefore, in addition to providing silicide source and drain structures, the present invention provides a more stable high-K gate dielectric layer by avoiding potentially damaging thermal processing.

The present invention recognizes that a problem exists with respect to the instability of high-K materials when a thermal budget for the high-K material is exceeded (e.g., due to anneal cycles associated with ion implantation to activate dopant species and/or recrystalize the implanted semiconductor material). Further, the present invention provides a solution to this problem.

Claim 1 calls for a semiconductor device, which includes a source and a drain, where the source and the drain consist essentially of silicide, and a gate dielectric made from a high-K material (i.e., a material having a relative permittivity of greater than 10).

Wilting fails to disclose or fairly suggest a semiconductor device, which includes a high-K gate dielectric. Paragraph 5 of the Office action states that, "there is a gate dielectric (4A, 4B), made from silicon oxide (4A) and silicon nitride (4B), which separates the gate electrode (16A) and the body."

At the outset, applicants note that neither silicon oxide nor silicon nitride, standing alone as a single layer or formed together as stacked layers, constitute a high-K gate dielectric, as defined by the applicant. In particular, silicon oxide has a K of approximately 3.9 (see, for example, page 5, lines 16-17 of the present application and Grant at col. 1, line 15), while silicon nitride has a K of approximately 6-9 (see, for example, page 5, lines 6-7 of the present application).

Claim 1 calls for a high-K gate dielectric, that is, a gate dielectric having a K of greater than 10, in one embodiment, and greater than 20 in another embodiment (see, for example, the present application at page 4, lines 18-24). In this regard, applicants respectfully remind the Examiner that pursuant to MPEP 2173.05(a), "when the specification states the meaning that a term in the claim is intended to have, the claim is examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art." *In re Zletz*, 893 F.2d 319, 13 USPQ.2d 1320 (Fed. Cir. 1989).

Further, the Office action's reliance on Lee for a showing that silicon oxide and silicon nitride (as used and disclosed by Wilting) are high-K materials is improper. First, at col. 5, lines 30-31, Lee does not discuss silicon oxide or silicon nitride. Rather, Lee discusses a "NO (Nitride-Oxide)" layer, which is not a conventional chemical expression and, at best, can be interpreted as silicon oxynitride, having a K of about 4-8. Second, even if Lee referred to one or both of silicon nitride and silicon oxide as "high-K materials," this characterization is irrelevant in light of applicants' clear enumeration of the meaning of the claim term within the specification of the application.

In addition, Wilting fails to disclose or fairly suggest a semiconductor device, which includes a source and a drain consisting essentially of silicide. Paragraph 5 of the Office

action points to col. 7, lines 46-47 of Wilting, alleging that Wilting "discloses that the source and drain regions (31, 32) are entirely silicide." However, applicants respectfully submit that this language is taken out of context. In particular, the description found at col. 7, lines 46-55 of Wilting describes Figure 16, which illustrates silicide drain zones (31) and (32) within p-type drain zones (41) and (42) (designated by dashed lines in Figures 14-16).

More particularly, Figures 14-16 of Wilting, along with the associated description in column 7, clearly differentiate between the source and drain zones (41) and (42) and source and source and drain zones (31) and (32). P-type source and drain zones (41) and (42) are formed by "indiffusion or implantation." (see, for example, col. 7, lines 49-50). For these reasons alone, claim 1 is neither anticipated nor rendered obvious by Wilting.

In addition, "a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified." MPEP 2141.02, *citing, In re Sponnoble*, 160 U.S.P.Q. 237, 243 (CCPA 1969). Applicants acknowledge that those who allege discovery of the source of a problem and solution must provide substantiating evidence. MPEP 2141.02.

In this case, applicants, at the time of the invention, discovered that a need exists for a semiconductor device having a stable, quality high-K dielectric layer that is not compromised (i.e., the thermal budget is not exceeded, causing the material becoming unstable, to lose its electrical characteristics, and/or to react undesirably with other materials in the device) due to thermal processing associated with anneal cycles following source and drain ion implantation.

Evidence of the discovery of the source or cause of this problem, i.e., instability of high-K materials when a thermal budget for the high-K material is exceeded (e.g., following anneal cycles to activate dopant species forming the source and/or drain), can be found in Applicant's Patent Application at page 10, lines 17-29.

Further, in response to the discovered problem, applicants developed a solution to the problem. A semiconductor device was created that includes a quality high-K dielectric layer, which is not compromised by additional thermal processing required by high

temperature anneal cycles following ion implantation. Rather, a device having a source and a drain consisting essentially of silicide is formed with low temperature processing (e.g., about 350°C to about 450°C) and without conventional ion implantation. These limitations, which solve the discovered problem, are present in claim 1 and distinguish the invention patentably over the references of record.

With regard to the alternate rejection of claim 1 (i.e., Grant in view of Wilting), both Grant (see, for example, col. 2, lines 41-44) and Wilting (see above discussion) teach sources and drains formed using conventional ion implantation. This ion implantation must be coupled with relatively high temperature processing (e.g., about 1000°C, as disclosed in Wilting), which is prone to damage an associated high-K gate dielectric layer. In contrast, the present invention discovered the source of a problem involving the thermal budget of high-K gate dielectric materials and provided a solution (i.e., a device having a silicide source and drain formed without ion implantation).

The other cited references, including Raajimakers et al. and Venkatesan et al., fail to cure the deficiencies of both Wilting and Grant. Accordingly, it is submitted that **claim 1** and **claims 2-10,** dependent therefrom, distinguish patentably over the references of record. In addition, the dependent claims recite additional novel and unobvious features of the invention.

Claim 20, which has been placed in independent form, calls for a semiconductor device including a source and a drain consisting essentially of silicide and a semiconductor body disposed between the source and the drain, wherein a **source/body junction is defined by silicide material of the source and semiconductor material of the body and a drain/body junction is defined by silicide material of the drain and semiconductor of the body**.

None of the cited references, taken alone or in combination, disclose or fairly suggest source/body and drain/body junctions defined by silicide material of the source/drain and semiconductor material of the body.

In this regard, applicants respectfully submit that what is alleged in paragraphs 9 and 16 of the Office action is simply inaccurate. In particular, both of paragraphs 9 and 16 of the Office action point to Figure 16 of Wilting for the teaching of source/body and drain/body junctions defined by silicide material of the source/drain and semiconductor material of the body. However, **Figure 16 of Wilting, along with the associated description at column 7, clearly shows silicide source zone (31) within implanted p-type source zone (41) (shown by dashed line) and silicide drain zone (32) within implanted p-type drain zone (42) (shown by dashed line)**. As such, the source/body junction of the device disclosed in Wilting is defined by the p-type semiconductor material of source zone (41) and the semiconductor material of the body. Similarly, the drain/body junction of the Wilting device is defined by the p-type semiconductor material of drain zone (42) and the semiconductor material of the body. Grant, along with the other cited references, fails to cure the deficiencies of Wilting.

Accordingly, it is submitted that **claim 20** distinguishes patentably over the references of record.

Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. §102(b) and §103(a) is requested.

Conclusion

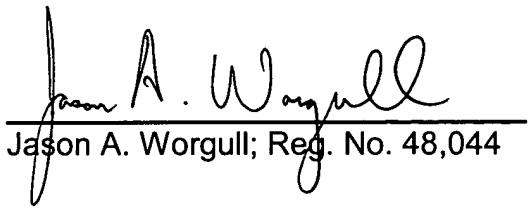
In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested.

If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any fees resulting from this communication, please charge same to our Deposit Account No. 18-0988, our Order No. G0615.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

By 
Jason A. Worgull; Reg. No. 48,044

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1621 Euclid Avenue
Nineteenth Floor
Cleveland, Ohio 44115
Telephone: (216) 621-1113
Facsimile: (216) 621-6165

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